

40 MBPS PMC BIT SYNCHRONIZER

BSZ532



The PCI Mezzanine Card (PMC) Bit Synchronizer (BSZ532) extracts and decodes data and clock from a potentially degraded input PCM data stream at rates up to 40 Mbps, while keeping bit error rates to within 1 dB of theoretical. It adapts to a wide range of input signal conditions using a combination of analog and digital techniques with automatic and host-selectable features. One of the most capable bit synchronizers on the market today, the BSZ532 runs at data rates of up to 40 Mbps for NRZ codes and 30 Mbps for bi-phase codes, with bit error rate performance to within 1.0 dB of theoretical across the entire operational range.

Over-sampled rates of at least four times the bit rate ensure an improved matched filter and therefore bit error rate (BER) performance - even in the high octave range. A new mixed-signal (analog and digital) phase-locked loop (including a direct digitally synthesized clock tracker) yields reliable and stable loop performance at all frequencies and up to 1.6% loop bandwidth. Digitally controlled automatic gain and offset circuits track amplitude and offset variations, ensuring minimal degradation of BER and optimal acquisition performance.

KEY FEATURES

- Achieves BER within 1.0 dB of theoretical over the entire operational range
- Selects any center frequency to within 0.1% at 100 bps to 40 Mbps for NRZ codes and to 30 Mbps for bi-phase codes
- Second-order phase-locked loop extracts a stable clock from noisy and distorted input signals
- Host-selectable loop bandwidth (LBW) from 0.1% to 1.6%
- Tracking range 3 x LBW
- Provides fast acquisition of new signals and retention during temporary signal dropouts
- Automatic gain and offset controls track amplitude and offset variations and rapidly adapt to signal changes
- Selects PCM source from the following inputs: two single-ended, one differential



Excellence You Can Measure

Telemetry & RF Products

40 MBPS PMC BIT SYNCHRONIZER

BSZ532 SPECIFICATIONS

Inputs

PCM	.2 single-ended, 1 differential (RS-422)
IRIG Code Formats	.NRZ-L/M/S, RNRZ-L, BiΦ-L/M/S
Derandomizer	.Forward or reverse sequence = $2n-1$ ($n=11, 15, 17$)
Bit Rate (all codes)	.100 bps to 40 Mbps (NRZ codes) .100 bps to 30 Mbps (Bi-phase codes)
AC Offset	.Up to 100% of signal amplitude at sinusoidal frequencies up to 0.05% of bit rate
Signal Range	.0.2 to 10V peak-to-peak
DC Common Mode Max.	. $\pm 6V$ (75 Ω impedance) . $\pm 10V$ (10 K Ω impedance)
Impedance	.10 K Ω (High) or 75 Ω (Low), programmable for single ended inputs (SRC1 or SRC2) 100 W for differential input

Performance

Bit Error Rate	.Within 1.0 dB of theoretical
Loop Bandwidth	.0.1%, 0.2%, 0.4%, 0.8%, 1.6%, programmable
Acquisition Range	. $\pm 2 \times$ LBW @ $E_b/N_0 \geq 12$ dB
Acquisition Time (avg.)	.NRZ: ≤ 100 bits @ $E_b/N_0 \geq 12$ dB BiF: ≤ 200 bits @ $E_b/N_0 \geq 12$ dB
Sync Retention (flywheel)	.Sync will be maintained for at least 128 bits at 0.1% LBW @ $E_b/N_0 \geq 12$ dB
Sync Threshold	. $E_b/N_0 \geq 0$ dB at 0.1% LBW
Tracking Range	. $\pm 3 \times$ LBW @ $E_b/N_0 \geq 12$ dB

Outputs

Differential (LVDS)	.8 programmable clock and data outputs to the PMC Mezzanine Carrier for distribution to a PMC Decom
Clock & Data	.TTL level, 50 Ω min. load
Data Format	.NRZ-L
Data Polarity	.Normal & inverted
Clock Phase	.0°, 180°
Tape	.TTL level, 50 Ω min. load
Codes	.NRZ-L/M/S, RNRZ-L, BiΦ-L/M/S
Randomizer	.Forward or reverse sequence = $2n-1$, where $n = 11, 15, 17$
Data Polarity	.Normal & inverted

Functions

Bit Synchronizer Type	.Second-order phase-locked loop
Tuning Resolution	.0.1%
Programming Resolution	.0.1% of bit rate
Status to Host (or display)	.Bit Sync Lock, Signal Detect

Options (contact factory)

Input Codes	.RZ, DM-M/S, M2
Soft Bit Decisions	.3 bits
Alternate Symbol	
Inversion FEC Modes	.None, Standard, 171-Inverted
Randomizer/Derandomizer	. $n = 20$, CCITT Recommendation V.35

Program Setup and Control

Keyboard and Mouse	.Displays with list-pick selections
ASCII Text File	.User-created description
API	.Application Programming Interface for remote setup (option)

General Requirements

System 550 or Avalon Chassis	.1 PMC slot
Rear Panel	.1 slot
4 BNC Connectors	.Source 1 & 2, clock & data
MDR-26	.All other inputs and outputs
Maximum per Chassis	.32 (550) / 20 (Avalon)
Power	.5V, +12V, -12V, 3.3V
Environment	.See datasheets for: Base 550 System Chassis (PRO550B), Avalon System Chassis (AVALON-R), VME Mezzanine Carrier (ZCM596), and VME Mezzanine Carrier with Arbiter (ZCA596)
Dimensions	.75mm x 150mm (PMC std.)

Compatibility

VME Mezzanine Carrier (ZCM596)	
VME Mezzanine Carrier with Arbiter (ZCA596)	
Standard PCI Carrier (sold as BSZ732-PCI)	
SWA500 Applications Software	
Vista Software (version 4.3.0 or higher for 40 Mbps operation; previous versions 30 Mbps)	

Ordering Information

BSZ532	.Bit Synchronizer Module, PMC (40 Mbps)
BSZ532-D	.Bit Synchronizer Module, PMC (40 Mbps), Differential

Telemetry-West

9020 Balboa Avenue

San Diego, CA 92123-3507

858.694.7500 800.351.8483

Fax: 858.279.0693

www.L-3Com.com/TW



Telemetry & RF Products

This technical data and software is considered as Technology Software Publicly Available (TSPA) as defined in Export Administration Regulations (EAR) Part 734.7-11. Specifications subject to change without notice. Call for latest revision. All brand names and product names referenced are trademarks, registered trademarks, or trade names of their respective holders. 7/09 ML 378 Rev J