

## PMC DECOMMUTATOR 30 MBPS

### DCZ534



#### KEY FEATURES

- Decommutes a serial data stream up to 30 Mbps
- Up to 4 PMC modules per MUXbus slot using VME Mezzanine Carriers\*
- Switches to one of 16 formats per module on operator command or on the format ID word
- Generates frame quality status words
- Offers a 3-bit frame sync aperture and up to 64 bits per frame sync word
- Aligns MSB or LSB on a word-by-word basis
- Includes up to 1,024 minor frames
- Provides independent frame and subframe data pass qualifiers
- Checks and/or strips parity (odd, even, off)
- Supports TTL or RS-422 inputs (DCZ534-D)

The PCI Mezzanine Card (PMC) Decommulator (DCZ534) is a multiformat PCM telemetry decom that is designed to meet the needs of the most demanding telemetry applications. It provides frame-synchronized instant format switching for up to 16 unique formats, a large aggregate major frame size to over 4 million words with minor frames to 65,536 words, and continuous data rates up to 30 Mbps.

The DCZ534 module generates a quality status word to report data integrity. In addition, it offers a flexible synchronization strategy and parity checking. The module can be set up via a GUI common to all system decoms, via an externally generated flat file, or via the system's API. Both the GUI and the API provide a means for continuous module status monitoring.

*Excellence You Can Measure*



### DCZ534 SPECIFICATIONS

#### Inputs

Data Rates .....10 bits/sec to 30 Mbps; 3.3 Mwords/sec  
 PCM Data Codes .....NRZ-L  
 Data Length .....Variable from 2 to 32 bits per word  
 Data Polarity .....Normal/inverted/auto (no auto with FCC/URC)  
 Data Alignment .....MSB/LSB first per word  
 Parity Location .....Last bit  
 Parity Stripping .....Strip/pass  
 CRC Check .....Enabled or disabled per bit  
 CRC Polynomial .....Any polynomial 4 to 32 bits, including CRC-12, LRC-8, CRC-16, CRC-16 Reverse, CRC-CCITT, CRC-CCITT Reverse, NASCOM, Ethernet, 32<sup>nd</sup>-order, POLY 1, POLY 2  
 Input Levels .....TTL (data/clock);  
 RS-422 (data/clock) (DCZ534D)  
 Clock Input Phase .....0 or 180°  
 Clock Duty Cycle .....50 ±10%

#### Outputs

Word format .....2- to 32-bit data, zero or sign extended to 32 bits, 16-bit tag  
**Data Pass Qualifiers**  
 Frame Sync .....Search, check, verify, or lock  
 Subframe Sync .....Search, check, verify, or lock  
 Parity .....Pass always or pass if good  
 Active Format .....Pass if format in memory  
 Parameter .....Pass if parameter selected for output

#### Formats

Format Size  
 Frames per Major Frame .....Up to 1,024 minor frames ‡

| Format(s)             | 1                   | 2                   | 3-4                 | 5-8                 | 9-16                |
|-----------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| Words per Major Frame | (4M) 4 to 4,194,304 | (2M) 4 to 2,097,152 | (1M) 4 to 1,048,576 | (512K) 4 to 524,228 | (256K) 4 to 262,144 |
| Words per Minor Frame | (64K) 4 to 65,536   | (64K) 4 to 65,536   | (64K) 4 to 65,536   | (64K) 4 to 65,536   | (64K) 4 to 65,536   |

‡ Subject to words per major frame limits

#### Format Switching Control

Memory Resident Formats .....Up to 16  
 Initiation .....On command; on format ID word  
 Format ID Word .....4 to 10 consecutive bits; fixed bit position in frame  
 Format Switching Boundary .....Right after the format ID word or at the end of the current minor frame  
 Format Variables .....Words per minor frame, word locations, bits per word, words per major frame, bits per minor frame  
 Format Constants .....Frame sync pattern, subframe sync pattern, subframe sync method, data polarity, format ID word position, format ID word length, frames per major frame

#### Frame Sync Characteristics

Frame Sync Pattern Length .....8 to 64 bits  
 Search-to-Lock .....1 to 16 valid sync words  
 Lock-to-Search .....1 to 16 invalid sync words  
 Error Threshold .....0 to 7 bits  
 Bit Slip Window .....0 to ±3 bits

#### Subframe Sync Characteristics

Subframe Sync Bits .....8 to 64 for FCC/URC; 4 to 10 for SFID  
 SFID Offset .....0 to 28 bits  
 Method .....SFID, URC, FCC, none  
 Search-to-Lock .....1 to 16 valid sync words  
 Lock-to-Search .....1 to 16 invalid sync words  
 Error Threshold .....0 to 7 bits for FCC/URC; 0 for SFID  
 Independent Subframes .....1 per decom; more with FPP or in second decom  
 Lock .....End of any minor frame with SFID or at the start of major frame (URC, FCC)

#### Status

Output to MUXbus .....Frame sync state, subframe sync state, polarity, clock detector, bit slip count, frame sync bit error status, active format, valid format, CRC status, input source

#### Other Characteristics

Frame Word Definition .....Variable length word position  
 FPP Algorithms .....Sub-subframe, tagged data, async embedded merge, and embedded time per IRIG-106

#### General Requirements

System 550 Chassis .....1 PMC slot  
 Rear Panel:  
 DCZ534 .....2 slots, 2 TTL clock/data (4 BNC coaxial)  
 .....1 slot, 2 TTL clock/data (4 BNC coaxial)  
 DCZ534-D .....2 slots, 1 RS-422 clock/data (2 triax)  
 Maximum per Chassis .....32 (550) / 16 (Avalon)  
 Power .....5V @ 1 A; 3.3V @ 1 A  
 Environment .....See data sheets  
 Base 550 System Chassis (PRO550A, PRO550B),  
 Avalon System Chassis (AVALON-R),  
 VME Mezzanine Carrier (ZCM596),  
 VME Mezzanine Carrier with Arbiter (ZCA596)  
 Dimensions .....75mm x 150mm (PMC std.)  
 Status Display .....8 LEDs

#### Compatibility

VME Mezzanine Carrier (ZCM596)  
 VME Mezzanine Carrier with Arbiter (ZCA596)  
 SWA500 Applications Software  
 Vista Software

#### Ordering Information

DCZ534 .....Decommutator Module PMC (30 Mbps)  
 DCZ534-D .....Decommutator Module PMC (30 Mbps), Differential

\*Subject to aggregate Carrier throughput limitations

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