

MULTIFUNCTION PCIe TELEMETRY MODULE

MFT-800



L-3's PCIe Multifunction Telemetry Module (MFT-800) builds on the success of our previous generation PCI Multifunction Telemetry Module (MFT733A-PCI) by including the same key functions as two bit sync, decom and simulator channels in one board with IRIG time input/output support. The MFT-800 is a PCI Express™ compliant telemetry board approximately half the size of the MFT733A-PCI with better than double the throughput performance. It provides a complete PCM telemetry system for 1 or 2 data streams, ideally suited for quick look applications, flight-line checkout systems, and portable configurations. A rich, robust, and proven set of embedded functions typically offload the host processor and can be applied to a wide variety of data communications solutions.

Both Bit Synchronizers provide 1 bps tuning resolution and support input rates to 30 Mbps with user programmable matched filtering. The user also has the ability to independently program the symbol timing, tracking range, automatic gain, and DC tracking loop bandwidths to optimize the link performance for their specific application.

Both Decoms support input interfaces from external I/O, the bit syncs or the simulators at 30 Mbps rates for 4-bits words and 40 Mbps rates for 8-bit words. The PCIe Multifunction Telemetry Module is designed to support IRIG Standard 106 Chapter 4 class I and II.

The Simulators provide high-resolution frequency programming and low jitter output for two independent PCM outputs at rates to 40 Mbps.

IRIG time synchronization and generation are supported via proprietary embedded digital processing that optimally acquires and tracks IRIG time signals and rejects noise. IRIG time functions are closely coupled with decommutation, providing high accuracy time tagging of input data with 1 microsecond resolution for both real-time or playback applications.

KEY FEATURES

- Dual stream design saves bus slots
- Bus-mastering DMA channels can support both input and output channels
- Extract clock and data from noisy PCM data streams at rates to 30 Mbps
- Decode, translate, or generate IRIG-A, -B, or -G time
- Time tag PCM input frames with 1 microsecond resolution synchronized to an external source or on-board TCXO
- Status tag PCM input frames, including sync state, bit slip, CRC error detection
- Extract two asynchronous embedded frames, or fully decommutate a primary and an embedded stream
- Simulate telemetry data and formats to 40 Mbps
- Viterbi decoder supporting 1/2 rates
- Numerous I/O for simultaneous support to external equipment. e.g. decryptors

Excellence You Can Measure



Telemetry - West

MULTIFUNCTION PCIe TELEMETRY MODULE

MFT-800 SPECIFICATIONS

Bit Synchronizers (x2)

Signal Range	.25 mV to 2.5 Vpp (Auto Range) Low Option 50 mV to 5 Vpp (Auto Range) Standard 100 mV to 10 Vpp (Auto Range) High Option
Codes	.NRZ-L, NRZ-M, NRZ-S, BiΦ-L, BiΦ-M, BiΦ-S, RZ, randomized NRZ-L (11, 15, 17)
Bit rate	.100 bps to 30 Mbps/15 Mbps (NRZ/Biphase Codes)
Tuning resolution	.1 bps
Symbol Timing Loop Bandwidth	.0.1% to 1.6% (percent of transition rate)
Bit Rate Tracking Range	.0.1% to 5% of Bit Rate
AGC Loop Bandwidth	.0.01% to 0.05% of Bit Rate
DC Tracking Loop Bandwidth	.0.01% to 0.05% of Bit Rate
Outputs	.Clock/Data with programmable phase/polarity
Output Drive/Termination	.TTL Compatible CMOS: +/-32mA typical 33 ohm series termination RS422: 4Vpp typical no load, 3Vpp 120 ohm load Standard for each channel, Rate = 1/2, K = 7 (Contact factory for other options)
Veterbi Decoders	
Impedance	.10 Kohm or 75 ohm programmable

Input Channels (Decommutators) (x2)

Inputs	
Input Termination	.CMOS: Hi Impedance RS422: 120 ohm load
Data rates	.> 30 Mbps with 4 bpw > 40 Mbps with 8 bpw average
Input code	.NRZ-L or randomized NRZ-L
Data polarity	.Normal/Inverted/Auto
Data alignment	.MSB/LSB first per stream
Input levels	.TTL (data/clock) or RS-422 (data/clock)
Clock input phase	.0° or 180°
Clock duty cycle	.50 ± 15%
Data Buffer	
PCM data pass qualifier	.Frame and subframe Check or Lock and per-word programmable in sorted or tag/data modes
Data buffers	.Two independent 64-kword double buffers
Format	.Telemetry, status, and time words sorted per application setup, tag-data, or pass-through
Buffer access method	.Bus-mastering DMA controllers or slave reads and interrupts
Other Outputs	
Data pass qualifier	.Frame and subframe Check or Lock and per word
Embedded data streams	.2 max.
Status to host	.Frame sync state, subframe sync state, frame search detector, subframe search detector, bit slip detector, CRC error detector, interrupt state, interrupt overrun, active buffer size, bit rate
Frame and Subframe Characteristics (Sorted Mode or Tag-Data)	
Sync pattern	.64 bits max.
Subframe sync method	.SFID, unique sync code, URC, FCC, or none
Search-to-lock	.1 to 4 valid sync words
Lock-to-search	.1 to 4 valid sync words
Error threshold	.0 to 3 bits
Sync aperture	.±0 or ±1 bit
Frame size	.4 to 65,536 telemetry words
CRC error checking	.Programmable polynomial and word location to 16th order
Time-Tagging (Sorted Mode)	
Time source	.Internal time clock optionally synchronized to external IRIG
Format	.BCD — microseconds to hundreds of days
Trigger source	.End of minor frames
Resolution	.One microsecond
Status Tagging (Sorted Mode)	
Trigger source	.End of minor frames

Output Channels (Simulators) (X2)

Modes of Operation	
Packed Data	.A single data buffer is bit packed at setup and continuously transmitted
Streaming	.Alternates between two data buffers under real-time host control
Burst	.Transmits one or two buffers of data and stops
Instruction	.Instructions and data are written at setup. Instructions specify the bpw, repeat count and jump command allowing the sequence to repeat
Data Buffer	
Packed Data	.8 Meg x 16 bits shared, programmable buffer sizes for each simulator

Streaming	.8 Meg x 16 bits shared, programmable buffer sizes for each simulator
Burst	.8 Meg x 16 bits shared, programmable buffer sizes for each simulator
Instruction	.4 Meg Instruction/Data Pairs shared
Outputs	
Data rates	.10 bps to 40 Mbps
Data rate resolution	.1 bps
Synthesizer Accuracy	.+/- 0.5 ppm
Time Base Accuracy	.Initial Error +/- 2 ppm Temperature Stability +/- 0.25 ppm Total Error +/- 4.6 ppm over 20 years
PCM data codes	.NRZ-L, NRZ-M, NRZ-S, BiΦ-L, BiΦ-M, BiΦ-S, RZ, randomized NRZ-L (11, 15, 17)
Outputs	.Clock/Data with programmable phase/polarity
Output drive/Termination	.CMOS: +/- 32 mA typical 33 ohm series termination RS422: 4 Vpp typical no load, 3 Vpp 120 ohm load
Clock output phase	.0° or 180°
Clock source	.Internal/external

Time Code Reader/Generator/Translator

Inputs (applies to Reader Mode only)	
Format	.Analog: IRIG-A, -B, or -G forward
Playback rates	.A&B: 1/4, 1/2, 1, 2, 4, 8, 16 G: 1/4, 1/2, 1, 2, 4, 8
Carrier frequency range	.±5% of nominal
Mark amplitude	.200 mV to 10V (auto-range)
Impedance	.10 kohm or 75 ohm programmable
Modulation ratio	.2:1 to 6:1
Error detection	.Error frame bypass option
Phase-locked-loop	.Tracks IRIG input time and generates time on signal loss
Internal Time Clock	
Modes of operation	.Translate or generate forward
Resolution	.One microsecond
Time Based Accuracy	.Initial Error Initial Error +/- 2 ppm, Temperature Stability +/- 0.25 ppm Total Error +/- 4.6 ppm over 20 years TCXO

Outputs

Format	.Analog: IRIG-A, -B, or -G Digital PWM with CMOS or RS422 driver
Amplitude/Source Termination	.1 to 10 Vpp no load, 75 ohm standard I/O source impedance
Modulation ratio	.3:1 nominal

Connectors and Cable Assembly Options

Rear panel	.DB-62 (female)
Single-Ended Cable	.2 Bit Sync Inputs, IRIG Input, IRIG Out, 8 programmable CMOS I/O
Differential Cable	.2 Bit Sync Inputs, IRIG Input, IRIG Out, 8 programmable RS-422 I/O
Expanded Cable	.2 Bit Sync Inputs (Differential Optional) IRIG Input 2 programmable analog outputs (e.g. IRIG Out or Simulator) 15 programmable CMOS I/O 10 programmable RS-422 I/O

Card Type

PCI Express	.Short Form Factor, X4 connector per PCIe CEM spec, 1 lane used
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Power

+3.3V supply	.2 A typical ± 5%
+12V supply	.500 mA typical ± 5%, Not including output loading

Ordering Information

MFT800	.PCIe Multifunction Telemetry Module,
MFT800-1	.Low Signal Range
MFT800-2	.High Signal Range
MFT800-G	.GPS receiver for IRIG time discipline and GPS data
MFT800-C	.Hardware CVSD decoding, 2 channels
MFT800-H	.High rate bit sync to 40 Mbps/20Mbps (NRZ/biphase)
MFT800-V	.Punctured codes, 2/3, 3/4, 4/5, 5/6, 6/7, 7/8
MFT800 Cabling Options:	
CBL-MFT800-SE	.Single-Ended Cable Assembly (Standard option)
CBL-MFT800-DIF	.Differential Cable Assembly
CBL-MFT800-EXP	.Expanded Cable Assembly

Telemetry-West

9020 Balboa Avenue

San Diego, CA 92123-3507

858.694.7500 800.351.8483

Fax: 858.279.0693

www.L-3Com.com/TW



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