

# Telemetry - West

## ANALOG & DIGITAL PORTS DAUGHTER CARD

### ADP800



#### KEY FEATURES

- Plug-in module fully compatible with MFT800
- Up to 16 analog outputs
- 12 bit digital to analog conversion
- Up to 18 digital I/O - individually programmable as inputs or outputs
- Fully independent analog and digital channel control
- Real-time sample rates to 50 ksps per channel
- Streaming data from host PC at up to 1.6M parameters/sec
- Accuracy to <math><0.1\%</math> with user calibration
- Short circuit and overvoltage protection
- Processing algorithms supported through look-up table
- Up to 6th order polynomial conversion built in
- Static masking and bit shifting support
- CVSD decoded outputs from up to 2 analog channels
- BIST includes Ramp/Sinewave test pattern
- Win 7 Driver API's and L-3 Vista software (option)

L-3's ADP800 PCIe Multifunction Telemetry Module now offers an option to provide analog and digital interface signals for data extracted from acquired data streams. The ADP800 is a daughtercard module designed as a tightly integrated plug-in module for the MFT800 and provides up to 16 analog and 18 digital interfaces.

The ADP800 provides outputs of data extracted from one or both of the PCM streams processed by the MFT800 or from either of the ADP800's direct inputs. Outputs may be processed by the ADP800 in real-time using look-up table or other methods to provide the customer with a convenient method for adapting the outputs to a variety of applications.

Typical applications for the ADP800 real-time outputs include strip chart recorders, analog meters, lamps, and discrete control circuits. ADP800 outputs may also be useful in real-time closed loop feedback applications due to the inherent ability to provide data outputs in real-time as it is received by the module.

In addition to real-time data, the ADP800 supports streaming data from the host CPU. This feature allows processed data to be output through the analog and digital outputs on the module. A typical application would allow data acquired by the MFT800 (and transferred to the host PC) to be streamed back to the ADP800 (from the host PC) as processed data for output from the analog and digital outputs. In this mode, the input data clock would be used to provide a synchronous output data clock for the analog and digital outputs.

Standard software support for the ADP800 includes Win 7 Driver API's. The module is also available with full support under L-3's Vista Applications software (Win 7).

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### ADP-800 SPECIFICATIONS

#### Analog Outputs

Channels	.16 single-ended
DA Resolution & Ranges	.12-bits, scaled to +/-2.5V, +/-5V, +/-10V, 0 to 5V, or 0 to 10V
Maximum Sample Rate	.50 kspcs per channel, 100 kspcs goal
Offset Error	<25 LSBs +/-10mV (w/o user calibration), <1 LSBs +/-2mV typical (w/optional factory calibration)
DC Gain Error	<25 LSBs +/-0.5% (w/o user calibration), <1 LSBs +/-0.1% typical (w/optional factory calibration)
Output Impedance	.50 ohms +/- 5%
Output Current	.Up to 10 mA
Output Protection	.Continuous short circuit to ground: +/-15 kV ESD and +/-TBD V Overvoltage
Reset Level	.Programmable, defaults to programmed mid-scale

#### Output Sampling Control

Sample Timing Modes	.1) Samples are sent to DAC as soon as the parameter is received and processed. 2) Programmable digital oscillator frequency locked to the average input sample rate per major frame. Free-running only supported. 3) Host streaming output sample rate is controlled by the input sample rate from the decom input stream.
Output Modes	.All samples are sent to DACs based on a trigger event 1) Disabled - no samples sent to DAC 2) Free-Running

#### DAC Inputs

Input Coding	.Offset Binary, 2's Complement
Input Source	.1) Decom parameters 2) On-board Streaming/Simulation parallel data (16 Channels) 3) Streaming Host control at up to 1.6 M parameters per second

#### Parameter Processing

Static Masking	.Bit logical AND
Static Bit Shifting	.Shift Left or Right up to 15-bits
Static Look-Up Table	.16-bit fully programmable table
Arithmetic Operations	.1) 1 multiply and 1 add/subtract 2) $C_0 + C_1 * X + C_2 * X^2 + C_3 * X^3 + C_4 * X^4 + C_5 * X^5 + C_6 * X^6$
Audio Decoding	.2 Channels of Continuous Variable Slope Delta modulation per IIRIG106-09 appendix F

#### Auxiliary Discrete I/O

Individually programmable as inputs or outputs with inversion control	
RS422 Channels	.18, Handled via an external adapter
CMOS Single-Ended Channels	.18
Output Modes	.1) Parallel Simulator or parameter data/clock strobe (data limited to contiguous 16-bits) 2) Internal DAC clock strobe 3) General purpose clock synthesizer output (2 Channels) 4) On-board 20 MHz TCXO reference

#### Host Streaming

Channels	.16
Modes	.Streaming - Alternates between two data buffers under real-time host control
Data Buffer	.Streaming - 1 Meg x 16 bits shared 64K channel 20 MHz TCXO reference and Master Oscillator

#### Time Base

Accuracy	.TCXO: Initial Error +/-2ppm, Stability +/-0.25ppm, Supply & Load +/-0.05ppm, Static Temp Hysteresis 0.4ppm, Total Error All Conditions +/-4.6ppm over 20 years Master Oscillator: +/-1.5ppm, Stability +/-7ppm, Aging 1st Year +/-3ppm, Aging 15 Years +/-10ppm, Total Error All Conditions +/-2-ppm over 15 years
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#### Power Consumption

TBD A @ 12V, output loading not included, TBD A @ 3.3V

#### Software Development

Windows 7, API and Driver running under L-3 TW Vista

#### BIST

Ramp/Sinewave test pattern output modes for BIST

#### Optional Upgrades (Future)

ADP800-D	.Dual Decom Support
ADP800-S	.Dual Simulator Support

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